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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/029,608	05/15/1998	NORIO FUKASAWA	980233	6285

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/029,608	FUKASAWA ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *109-112,115,116,119,120,123,127 and 129-135* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *109-112,115,116,119,120,123,127 and 129-135* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5-6-3 has been entered.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 132 and 133 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

The non-described subject matter is the claim 132 negative limitation, "wherein no electronic circuit is formed on a back surface of the semiconductor element."

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 109-112, 131, 134 and 135 are rejected under 35 U.S.C. 102(e) as being anticipated by Yasunaga (5656863).

At column 1, line 1 to column 2, line 5, column 2, lines 37-57, column 3, lines 7-47, column 16, line 16 to column 18, line 12, and column 25, lines 44-47, Yasunaga teaches the following:

109. A semiconductor device comprising: a semiconductor element 113 having a surface on which protruding electrodes 112 are formed; a resin layer 111 formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof, said end portions protruding a height from the resin layer; and external connection protruding

electrodes 53b provided to the end portions of the protruding electrodes that protrude from the resin layer, said external connection protruding electrodes forming a bump, said bump having a height larger than said height of said protruding electrode protruding beyond said resin layer.

110. The semiconductor device as in 109 wherein both a side portion of the resin layer 121 and a side 109, portion of the semiconductor element 125 are respectively exposed.

111. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes having convex end portions are formed; a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except the convex end portions thereof, said convex end portions protruding a height from the resin layer; and external connection protruding electrodes provided to the convex end portions of the protruding electrodes that protrude from the resin layer, said external connection protruding electrodes forming a bump, said bump having a height larger than said height of said protruding electrode protruding beyond said resin layer.

112. The semiconductor device as in 111, wherein both of a side portion of the resin layer 121 and a side portion of the semiconductor element 125 are respectively exposed.

131. A semiconductor device comprising: a semiconductor element 3 having a surface on which protruding electrodes 9, 10 are formed; a compression-molded resin layer 1 formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof ("top surface of the first conductor 9"); and external connection protruding electrodes 10 provided to the end portions of the protruding electrodes that protrude from the compression-molded resin layer, the compression-molded resin layer and the semiconductor element having surfaces.

134. The semiconductor device as in 109, wherein said resin layer is a compression-molded layer.

135. The semiconductor device as in 111, wherein said resin layer is a compression-molded layer.

To further clarify the teaching of the process limitation, "wherein said resin layer is a compression-molded resin layer," the product of Yasunaga inherently possesses the structural characteristics imparted by this process limitation. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

Claims 115, 116, 119 and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Karnezos (4813129) and Yasunaga (5656863).

At column 5, line 42 to column 7, line 27, Karnezos teaches the following:

115. A semiconductor device comprising: a semiconductor element 12 having a surface on which electrode pads ["contact pads"] connected to an internal part of the semiconductor element and protruding electrodes 16c to be connected to an external part are formed; lead lines 46c each connecting one of the electrode pads ["traces terminating at contact pads"] and one of the protruding electrodes so that the protruding electrodes and the internal pad are connected through the lead lines; and a resin layer 42c formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof, the protruding electrodes having a core portion 18c and an electrically conductive film 20c formed on a surface of the core portion, the core portions of the protruding electrodes are directly formed on the lead lines, wherein the core portion comprises an elastic resin.

116. The semiconductor device as in 115: wherein the elastic resin is polyimide.

119. A semiconductor device comprising: a semiconductor element 12 having a surface on which electrode pads ["contact pads"] connected to an internal part of the semiconductor element and protruding electrodes 16c to be connected to an external part

are formed; lead lines 46c each connecting one of the electrode pads ["traces terminating at contact pads"] and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and an insulating layer 42c formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof; and external connection protruding electrodes 50c provided to the end portions of the protruding electrodes that protrude from the resin layer, the protruding electrodes having a core portion 18c and an electrically conductive film 20c formed on a surface of the core portion, the core portions of the protruding electrodes are directly formed on the lead lines, wherein the core portion comprises an elastic resin, and a part of said protruding electrode sealed by said resin layer and said end portions are covered commonly with said electrically conductive film.

120. The semiconductor device as in 119, wherein the elastic resin is polyimide.

To further clarify the teaching that the electrode pads are connected to an internal part of the semiconductor element and the protruding electrodes and the internal part are connected through the lead lines, it is noted that it is inherent that the semiconductor element comprises an internal part, and the pads,

internal part, protruding electrodes, and lead lines are at least physically connected to each other.

To further clarify the teaching that a part of said protruding electrode sealed by said resin layer and said end portions are covered commonly with said electrically conductive film, it is noted that the scope of the limitation is not limited to an embodiment wherein the part of the electrode sealed by the resin is in direct contact with the electrically conductive film.

However, Karnezos does not appear to explicitly teach that the insulating layer 42c is a resin layer.

Notwithstanding, at column 32, lines 27-44, Yasunaga teaches a resin insulating layer 1. In addition, it would have been obvious to combine the product of Yasunaga with the product of Karnezos because it would provide an insulating layer.

Claims 123, 127, 129 and 130 are rejected under 35 U.S.C. 102(b) as being anticipated by Brooks (5824569).

At column 1, lines 20-24, and column 2, line 29 to column 4, line 61, Brooks teaches the following:

127. A semiconductor device comprising: a semiconductor element 104 having a surface on which protruding electrodes 130 are formed; and a molded resin layer 110 formed on the surface of the semiconductor element so as to seal the protruding

electrodes except end portions thereof, wherein the molded resin layer and the semiconductor element have the structure of surfaces defined by cutting using a dicer ["segmented using a saw blade"].

123. A semiconductor device as in 127 wherein a part of a side portion of the semiconductor element being covered with the resin layer, a part of a side portion of said semiconductor element being exposed.

129. The semiconductor device as in 127 wherein a side surface of the resin layer and a side surface of the semiconductor device are flush with each other.

130. The semiconductor device as in 127, wherein end portions of the protruding electrodes protrude from the molded resin layer.

Also, although Brooks does not appear to explicitly teach the process limitation "compression-molded," the product of Brooks inherently possesses the structural characteristics imparted by the process limitation. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

Claims 132 and 133 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks (5824569).

As cited supra, in a first embodiment, Brooks teaches the following:

132. A semiconductor device characterized by comprising: a semiconductor element 30 having protruding electrodes 32 formed on a surface thereof: a first resin layer 36B that is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; and a second passivation layer 36A provided so as to cover at least a back surface of the semiconductor element, wherein the surface of the semiconductor element is formed with an electronic circuit [32 and "bond pad,"] and wherein no electronic circuit is formed on a back surface of the semiconductor element.

133. A semiconductor device as in 132, wherein a sidewall surface of said first passivation layer and a sidewall surface of said second passivation layer form a flush surface with said sidewall surface of said semiconductor element.

However, in the first embodiment, Brooks does not appear to explicitly teach a sidewall surface of said semiconductor element being exposed at a sidewall surface of said semiconductor device.

Regardless, as cited, in a second embodiment, Brooks teaches a sidewall surface of a semiconductor element 104 being exposed at a sidewall surface of the semiconductor device. In addition, it would have been obvious to combine the second

embodiment of Brooks with the first embodiment because it would facilitate mass production.

Applicant's amendment and remarks filed 5-6-3 have been fully considered, are addressed in the rejection supra, and are further addressed infra.

Applicant contends that Yasunaga does not teach that the bump has a height larger than the height of the protruding electrode protruding beyond the resin layer.

This contention is respectfully traversed because, as elucidated in the rejection, Yasunaga teaches this limitation. See especially Figure 101B.

Applicant also asserts, "there is no motivation in Karnezos to use the lead line for securing distance between the protruding core and the contact pad."

This assertion is respectfully traversed because the claims are not so limited, and Karnezos is not applied to the rejection for this teaching.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/308-7722.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
1-Jun-03